Supplemental Form PTO-1449 (Modified) LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary) Page 1 of 1	Attorney Docket No.: FIS920030187US1	Serial No.: 10/605,310
	Applicant: Dureseti Chidambarrao, et al.	
	Filing Date: September 22, 2003	Group: 2815

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINERS INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
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OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

PD			Kern Rim, et al., "Transconductance Enhancement in Deep Submicron Strained-Si *n*-MOSFETs", International Electron Devices Meeting, 26, 8, 1, IEEE, September 1998.
			Kern Rim, et al., "Characteristics and Device Design of Sub-100 nm Strained Si N- and PMOSFETs", 2002 Symposium On VLSI Technology Digest of Technical Papers, IEEE, pp 98-99.
			Gregory Scott, et al., "NMOS Drive Current Reduction Caused by Transistor Layout and Trench Isolation Induced Stress", International Electron Devices Meeting, 34.4.1, IEEE, September 1999.
			F. Ootsuka, et al., "A Highly Dense, High-Performance 130nm node CMOS Technology for Large Scale System-on-a-Chip Application", International Electron Devices Meeting, 23.5.1, IEEE, April 2000.
			Shinya Ito, et al., "Mechanical Stress Effect of Etch-Stop Nitride and its Impact on Deep Submicron Transistor Design", International Electron Devices Meeting, 10.7.1, IEEE, April 2000.
			A. Shimizu, et al., "Local Mechanical-Stress Control (LMC): A New Technique for CMOS-Performance Enhancement", International Electron Devices Meeting, IEEE, March 2001.
PD			K. Ota, et al., "Novel Locally Strained Channel Technique for high Performance 55nm CMOS", International Electron Devices Meeting, 2.2.1, IEEE, February 2002.

EXAMINER	PHUC T. DANG	DATE CONSIDERED	11/12/2004

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FORM PTO-1449 (Modified)	ATTY. DOCKET NO. FIS920030187US1	SERIAL NO. 10/605,310
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	APPLICANT: Chidambarrao, Dureseti, et al.	
(Use several sheets if necessary) DEC 0 5 2003	FILING DATE: 9/22/03	GROUP: Unassigned 2818

REFERENCE DESIGNATION — U.S. PATENT DOCUMENTS

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PD	US 6,228,694 B1	5/8/2001	Doyle et al.			
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INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
FIS920030187US1	10/605,310
Applicant(s)	
Chidambarrao, Dureseti, et al.	
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9/22/03	Unassigned

U.S. PATENT DOCUMENTS

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OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

PD		Novel Locally Strained Channel Technique for High Performance 55nm CMOS K. Ota, et al. 2002 IEEE, 2.2.1-2.2.4, IEDM 27. Local Mechanical-Stress Control (LMC): A New Technique for CMOS - Performance Enchancement A. Shimizu, et al. 2001 IEEE, 19.4.1-19.4.4, IEDM 01-433
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Chidambarrao, Dureseti, et al.	
Filing Date	**Group Art Unit**
9/22/03	~~Unassigned~~ 2819

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PD		NMOS Drive Current Reduction Caused by Transistor-Layout and Trench Isolation Induced Stress Gregory Scott, et al. 1999 IEEE, 34.4.1-34.4.4, IEDM 99-827 Transconductance Enhancement in Deep Submicron Strained-Si n- MOSFETs Kern (Ken) Rim, et al. 1998 IEEE, 26.8.1-26.8.4, IEDM 98-707
PD		Characteristics and Device Design of Sub-100 nm Strained Si N- and PMOSFET's K. Rim, et al. 2002 IEEE, 98-99, 2002 Symposium On VLSI Technology Digest of Technical Papers

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